

**SYNTHESIS CONFIGURATION CHART**

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_

DATE \_\_\_\_\_ FILE DATE \_\_\_\_\_

**SOFTWARE**

Software DIP Switch                      00 / 10 / 40 / 90

FmRt:            15            24            30

PIDn:           1:1           1:2

QCmp:           ON           OFF

Ssrc:           <none>    COM1    TC-560

PSrc:           \*

PFrq:           \*

Trml:           COM1    COM2

Prnt:           File:    COM1    COM2    COM3    COM4

Com1: \_\_\_\_\_

Com2: \_\_\_\_\_

Com3: \_\_\_\_\_

Com4: \_\_\_\_\_

Cons:           <none>    TR I    TR II

Port:           0378

Mstr:	1	2	3	4	5	6	7	8
	9	10	11	12	13	14	15	16

Xmit:           <none>    OLD 422    parllel    DMX/ESL    DMX/TRX    ANCOR

LtBs: \_\_\_\_\_

xTComA:       <none>    COM1    COM2    COM3    COM4

dGrp: \_\_\_\_\_

AnBs: \_\_\_\_\_

TComB:       <none>    COM1    COM2    COM3    COM4

dgrp: \_\_\_\_\_

anBs: \_\_\_\_\_

An B1 \_\_\_\_\_

An B2 \_\_\_\_\_

An B3 \_\_\_\_\_

An B4 \_\_\_\_\_

Di G1 \_\_\_\_\_

Di G2 \_\_\_\_\_

### CTU CONFIGURATION CHART

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_ ROM VER. \_\_\_\_\_  
 DATE \_\_\_\_\_ SERIAL # \_\_\_\_\_ BOARD RV \_\_\_\_\_

#### HARDWARE

JP2 COM2: Serial Protocol [1-2] RS-232 [2-3] RS-422  
 JP3 Clock Speed Vertical / Horizontal (Only on boards before Rev C)  
 JP4 Address Space 1 2 3 4 5  
*Normally [2-3] and [4-5]*

#### SOFTWARE

Software DIP Switch 00 / 10 / 40 / 90

Location

Frame: F0 F1  
 Format: CTU STU

ABANK1 A0 A1 A2 A3 A4 A5 A6 A7  
 A8 A9 AA AB AC AD AE AF

AOFST1 \_\_\_\_\_

ABANK2 A0 A1 A2 A3 A4 A5 A6 A7  
 A8 A9 AA AB AC AD AE AF

DBANK D0 D1

DSHIFT 0 1 2 3 4 5 6 7

DICHAN 16 24 32

REM A0 \_\_\_\_\_ A8 \_\_\_\_\_ D0 \_\_\_\_\_  
 A1 \_\_\_\_\_ A9 \_\_\_\_\_ D1 \_\_\_\_\_  
 A2 \_\_\_\_\_ AA \_\_\_\_\_ D2 \_\_\_\_\_  
 A3 \_\_\_\_\_ AB \_\_\_\_\_ D3 \_\_\_\_\_  
 A4 \_\_\_\_\_ AC \_\_\_\_\_  
 A5 \_\_\_\_\_ AD \_\_\_\_\_  
 A6 \_\_\_\_\_ AE \_\_\_\_\_  
 A7 \_\_\_\_\_ AF \_\_\_\_\_

**ANALOGS: 1 TO 32**

1	Name: _____	Mode _____	Trim: _____
2	Name: _____	Mode _____	Trim: _____
3	Name: _____	Mode _____	Trim: _____
4	Name: _____	Mode _____	Trim: _____
5	Name: _____	Mode _____	Trim: _____
6	Name: _____	Mode _____	Trim: _____
7	Name: _____	Mode _____	Trim: _____
8	Name: _____	Mode _____	Trim: _____
9	Name: _____	Mode _____	Trim: _____
10	Name: _____	Mode _____	Trim: _____
11	Name: _____	Mode _____	Trim: _____
12	Name: _____	Mode _____	Trim: _____
13	Name: _____	Mode _____	Trim: _____
14	Name: _____	Mode _____	Trim: _____
15	Name: _____	Mode _____	Trim: _____
16	Name: _____	Mode _____	Trim: _____
17	Name: _____	Mode _____	Trim: _____
18	Name: _____	Mode _____	Trim: _____
19	Name: _____	Mode _____	Trim: _____
20	Name: _____	Mode _____	Trim: _____
21	Name: _____	Mode _____	Trim: _____
22	Name: _____	Mode _____	Trim: _____
23	Name: _____	Mode _____	Trim: _____
24	Name: _____	Mode _____	Trim: _____
25	Name: _____	Mode _____	Trim: _____
26	Name: _____	Mode _____	Trim: _____
27	Name: _____	Mode _____	Trim: _____
28	Name: _____	Mode _____	Trim: _____
29	Name: _____	Mode _____	Trim: _____
30	Name: _____	Mode _____	Trim: _____
31	Name: _____	Mode _____	Trim: _____
32	Name: _____	Mode _____	Trim: _____

**ANALOGS: 33 TO 64**

33	Name: _____	Mode _____	Trim: _____
34	Name: _____	Mode _____	Trim: _____
35	Name: _____	Mode _____	Trim: _____
36	Name: _____	Mode _____	Trim: _____
37	Name: _____	Mode _____	Trim: _____
38	Name: _____	Mode _____	Trim: _____
39	Name: _____	Mode _____	Trim: _____
40	Name: _____	Mode _____	Trim: _____
41	Name: _____	Mode _____	Trim: _____
42	Name: _____	Mode _____	Trim: _____
43	Name: _____	Mode _____	Trim: _____
44	Name: _____	Mode _____	Trim: _____
45	Name: _____	Mode _____	Trim: _____
46	Name: _____	Mode _____	Trim: _____
47	Name: _____	Mode _____	Trim: _____
48	Name: _____	Mode _____	Trim: _____
49	Name: _____	Mode _____	Trim: _____
50	Name: _____	Mode _____	Trim: _____
51	Name: _____	Mode _____	Trim: _____
52	Name: _____	Mode _____	Trim: _____
53	Name: _____	Mode _____	Trim: _____
54	Name: _____	Mode _____	Trim: _____
55	Name: _____	Mode _____	Trim: _____
56	Name: _____	Mode _____	Trim: _____
57	Name: _____	Mode _____	Trim: _____
58	Name: _____	Mode _____	Trim: _____
59	Name: _____	Mode _____	Trim: _____
60	Name: _____	Mode _____	Trim: _____
61	Name: _____	Mode _____	Trim: _____
62	Name: _____	Mode _____	Trim: _____
63	Name: _____	Mode _____	Trim: _____
64	Name: _____	Mode _____	Trim: _____

**LDC CONFIGURATION CHART**

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_ ROM VER. \_\_\_\_\_  
 DATE \_\_\_\_\_ SERIAL # \_\_\_\_\_ BOARD RV \_\_\_\_\_  
 EVENT FILE \_\_\_\_\_ CUE FILE \_\_\_\_\_

**HARDWARE**

JP2 COM2: Serial Protocol [1-2] RS-232 [2-3] RS-422  
 JP3 Clock Speed Vertical / Horizontal (Only on boards before Rev C)  
 JP4 Address Space 1 2 3 4 5  
*Normally [2-3] and [4-5]*

**SOFTWARE**

Software DIP Switch 00 / 10 / 40  
 Number of Analog Channels 16 / 0  
 Number of Digital Channels 16 / 24 / 32  
 Frame Rate 15 / 30

	BAUD					DATA	PARITY	STOP BIT
<b>TERM</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>DATA</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 11</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 12</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 13</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 14</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 15</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 16</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 17</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>COM 18</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2

\* Denotes default configuration

## STU CONFIGURATION CHART

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_ ROM VER. \_\_\_\_\_  
 DATE \_\_\_\_\_ SERIAL # \_\_\_\_\_ BOARD RV \_\_\_\_\_

### HARDWARE

JP2 COM2: Serial Protocol [1-2] RS-232 [2-3] RS-422  
 JP3 Clock Speed Vertical / Horizontal (Only on boards before Rev C)  
 JP4 Address Space 1 2 3 4 5  
*Normally [2-3] and [4-5]*

### SOFTWARE

Software DIP Switch 00 / 10 / 40 / 90

Location

Name:

Frame:	F0	F1							
Format:	CTU	STU							

ABANK1	A0	A1	A2	A3	A4	A5	A6	A7
	A8	A9	AA	AB	AC	AD	AE	AF

AOFST1 \_\_\_\_\_

ABANK2	A0	A1	A2	A3	A4	A5	A6	A7
	A8	A9	AA	AB	AC	AD	AE	AF

DBANK	D0	D1						
-------	----	----	--	--	--	--	--	--

DSHIFT	0	1	2	3	4	5	6	7
--------	---	---	---	---	---	---	---	---

DICHAN	16	24	32					
--------	----	----	----	--	--	--	--	--

POT	1 _____	2 _____	3 _____	4 _____
-----	---------	---------	---------	---------

SWITCH	1 _____	2 _____	3 _____	4 _____
	5 _____	6 _____	7 _____	8 _____

MAX SERVO \_\_\_\_\_

WAKE CHAN: \_\_\_\_\_

**STU ANALOG SETUP**

	Name	Low	Hi	Rfbk	Xfbk	Beg	Ofs	Pol	Enb	Gain	Int	Drv
1												
2												
3												
4												
5												
6												
7												
8												
9												
10												
11												
12												
13												
14												
15												
16												
17												
18												
19												
20												
21												
22												
23												
24												
25												
26												
27												
28												
29												
30												
31												
32												

## DTU CONFIGURATION CHART

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_ ROM VER. \_\_\_\_\_  
 DATE \_\_\_\_\_ SERIAL # \_\_\_\_\_ BOARD RV \_\_\_\_\_

### HARDWARE

JP2	COM2: Serial Protocol	[1-2] RS-232	[2-3] RS-422
JP3	Clock Speed	Vertical / Horizontal	(Only on boards before Rev C)
JP4	Address Space	1    2    3    4    5	

*Normally [2-3] and [4-5]*

### SOFTWARE

Software DIP Switch                      00 / 10 / 40 / 90

Location

Name:

Frame:	F0	F1							
Format:	CTU	STU							

ABANK1	A0	A1	A2	A3	A4	A5	A6	A7
	A8	A9	AA	AB	AC	AD	AE	AF

AOFST1

ABANK2	A0	A1	A2	A3	A4	A5	A6	A7
	A8	A9	AA	AB	AC	AD	AE	AF

DBANK	D0	D1						
-------	----	----	--	--	--	--	--	--

DSHIFT	0	1	2	3	4	5	6	7
--------	---	---	---	---	---	---	---	---

DICHAN	16	24	32					
--------	----	----	----	--	--	--	--	--

## BART CONFIGURATION CHART

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_ ROM VER. \_\_\_\_\_  
 DATE \_\_\_\_\_ SERIAL # \_\_\_\_\_ BOARD RV \_\_\_\_\_  
 EVENT FILE \_\_\_\_\_ CUE FILE \_\_\_\_\_

### HARDWARE

JP2	75 ohm Termination	ON / OFF	
JP13	Sync Mode	[1-2] PILOT	[2-3] SMPTE
JP7	SER C Protocol	[1-2] RS-232	[2-3] RS-485 (and RS-422)
JP8	SER D Protocol	[1-2] RS-232	[2-3] RS-485 (and RS-422)
JP9	Digital Out +12	ON / OFF	
JP10	Digital Out Ground	ON / OFF	
JP11	Digital In +12	ON / OFF	
JP12	Digital In Ground	ON / OFF	
JP3	(DO NOT MOVE)	[2-3]	
JP4	(DO NOT MOVE)	[1-2]	
JP14	(DO NOT MOVE)	[1-2]	
TC-336	Analog Card	YES / NO	
	JP-1 (Uni/Bi)	[1-2] [2-3]	
	JP-2 (Uni/Bi)	[1-2] [2-3]	

### SOFTWARE

Software DIP Switch            00 / 10 / 40  
 Number of Analog Channels    16 / 0  
 Number of Digital Channels    16 / 24 / 32

	BAUD					DATA	PARITY	STOP BIT
<b>SER A [TERM]</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>SER B [COM 3]</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>SER C [DATA]</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2
<b>SER D [COM4]</b>	2400	4800	*9600	38.4k	Extern	7 *8	*N E O	*1 2

\* Denotes default configuration

## TC-560 TRANSMITTER CARD CONFIGURATION CHART

PROJECT \_\_\_\_\_ LOCATION \_\_\_\_\_ ROM VER. \_\_\_\_\_  
DATE \_\_\_\_\_ SERIAL # \_\_\_\_\_ BOARD RV \_\_\_\_\_

### HARDWARE

JP3	Sync Mode	[1-2] PILOT	[2-3] SMPTE
JP8	Address Select	[1-2] / *[2-3]	
JP2	IRQ	[1-2] / [2-3] / *[OFF]	
JP4	N/A	[1-2] / [2-3] / *[OFF]	
JP5	N/A	[1-2] / [2-3] / *[OFF]	

*\* Denotes default configuration*

### SOFTWARE

Software DIP Switch                    00 / 10 / 40 / 90

Format:                    CTU        STU        ESL

Sync                    Internal    SMPTE    Pilot    Remote    Sx = \_\_\_\_\_

Txd = \_\_\_\_\_

X = \_\_\_\_\_

**CPU EVENTS SUBROUTINES**

0		51		102		153		204
1		52		103		154		205
2		53		104		155		206
3		54		105		156		207
4		55		106		157		208
5		56		107		158		209
6		57		108		159		210
7		58		109		160		211
8		59		110		161		212
9		60		111		162		213
10		61		112		163		214
11		62		113		164		215
12		63		114		165		216
13		64		115		166		217
14		65		116		167		218
15		66		117		168		219
16		67		118		169		220
17		68		119		170		221
18		69		120		171		222
19		70		121		172		223
20		71		122		173		224
21		72		123		174		225
22		73		124		175		226
23		74		125		176		227
24		75		126		177		228
25		76		127		178		229
26		77		128		179		230
27		78		129		180		231
28		79		130		181		232
29		80		131		182		233
30		81		132		183		234
31		82		133		184		235
32		83		134		185		236
33		84		135		186		237
34		85		136		187		238
35		86		137		188		239
36		87		138		189		240
37		88		139		190		241
38		89		140		191		242
39		90		141		192		243
40		91		142		193		244
41		92		143		194		245
42		93		144		195		246
43		94		145		196		247
44		95		146		197		248
45		96		147		198		249
46		97		148		199		250
47		98		149		200		251
48		99		150		201		252
49		100		151		202		253
50		101		152		203		254

\* 255 is reserved for wildcards

**CPU TRIGGER NUMBERS**

0	51		102		153		204
1	52		103		154		205
2	53		104		155		206
3	54		105		156		207
4	55		106		157		208
5	56		107		158		209
6	57		108		159		210
7	58		109		160		211
8	59		110		161		212
9	60		111		162		213
10	61		112		163		214
11	62		113		164		215
12	63		114		165		216
13	64		115		166		217
14	65		116		167		218
15	66		117		168		219
16	67		118		169		220
17	68		119		170		221
18	69		120		171		222
19	70		121		172		223
20	71		122		173		224
21	72		123		174		225
22	73		124		175		226
23	74		125		176		227
24	75		126		177		228
25	76		127		178		229
26	77		128		179		230
27	78		129		180		231
28	79		130		181		232
29	80		131		182		233
30	81		132		183		234
31	82		133		184		235
32	83		134		185		236
33	84		135		186		237
34	85		136		187		238
35	86		137		188		239
36	87		138		189		240
37	88		139		190		241
38	89		140		191		242
39	90		141		192		243
40	91		142		193		244
41	92		143		194		245
42	93		144		195		246
43	94		145		196		247
44	95		146		197		248
45	96		147		198		249
46	97		148		199		250
47	98		149		200		251
48	99		150		201		252
49	100		151		202		253
50	101		152		203		254

\* 255 is reserved for wildcards

**CPU X VARIABLES**

0		32	
1		33	
2		34	
3		35	
4		36	
5		37	
6		38	
7		39	
8		40	
9		41	
10		42	
11		43	
12		44	
13		45	
14		46	
15		47	
16		48	
17		49	
18		50	
19		51	
20		52	
21		53	
22		54	
23		55	
24		56	
25		57	
26		58	
27		59	
28		60	
29		61	
30		62	
31		63	

**LDC/BART EVENTS SUBROUTINES**

0	51	102	153	204
1	52	103	154	205
2	53	104	155	206
3	54	105	156	207
4	55	106	157	208
5	56	107	158	209
6	57	108	159	210
7	58	109	160	211
8	59	110	161	212
9	60	111	162	213
10	61	112	163	214
11	62	113	164	215
12	63	114	165	216
13	64	115	166	217
14	65	116	167	218
15	66	117	168	219
16	67	118	169	220
17	68	119	170	221
18	69	120	171	222
19	70	121	172	223
20	71	122	173	224
21	72	123	174	225
22	73	124	175	226
23	74	125	176	227
24	75	126	177	228
25	76	127	178	229
26	77	128	179	230
27	78	129	180	231
28	79	130	181	232
29	80	131	182	233
30	81	132	183	234
31	82	133	184	235
32	83	134	185	236
33	84	135	186	237
34	85	136	187	238
35	86	137	188	239
36	87	138	189	240
37	88	139	190	241
38	89	140	191	242
39	90	141	192	243
40	91	142	193	244
41	92	143	194	245
42	93	144	195	246
43	94	145	196	247
44	95	146	197	248
45	96	147	198	249
46	97	148	199	250
47	98	149	200	251
48	99	150	201	252
49	100	151	202	253
50	101	152	203	254

\* 255 is reserved for wildcards

**LDC TRIGGER NUMBERS**

0		51		102		153		204
1		52		103		154		205
2		53		104		155		206
3		54		105		156		207
4		55		106		157		208
5		56		107		158		209
6		57		108		159		210
7		58		109		160		211
8		59		110		161		212
9		60		111		162		213
10		61		112		163		214
11		62		113		164		215
12		63		114		165		216
13		64		115		166		217
14		65		116		167		218
15		66		117		168		219
16		67		118		169		220
17		68		119		170		221
18		69		120		171		222
19		70		121		172		223
20		71		122		173		224
21		72		123		174		225
22		73		124		175		226
23		74		125		176		227
24		75		126		177		228
25		76		127		178		229
26		77		128		179		230
27		78		129		180		231
28		79		130		181		232
29		80		131		182		233
30		81		132		183		234
31		82		133		184		235
32		83		134		185		236
33		84		135		186		237
34		85		136		187		238
35		86		137		188		239
36		87		138		189		240
37		88		139		190		241
38		89		140		191		242
39		90		141		192		243
40		91		142		193		244
41		92		143		194		245
42		93		144		195		246
43		94		145		196		247
44		95		146		197		248
45		96		147		198		249
46		97		148		199		250
47		98		149		200		251
48		99		150		201		252
49		100		151		202		253
50		101		152		203		254

\* 255 is reserved for wildcards

### LDC/BART X VARIABLES

0		32	
1		33	
2		34	
3		35	
4		36	
5		37	
6		38	
7		39	
8		40	
9		41	
10		42	
11		43	
12		44	
13		45	
14		46	
15		47	
16		48	
17		49	
18		50	
19		51	
20		52	
21		53	
22		54	
23		55	
24		56	
25		57	
26		58	
27		59	
28		60	
29		61	
30		62	
31		63	